

<b>Notice of References Cited</b>	Application/Control No. 09/917,661	Applicant(s)/Patent Under Reexamination PARVATHALA ET AL.	
	Examiner John J. Tabone, Jr.	Art Unit 2133	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Shen et al., Native Mode Functional Test Generation for Processors with Applications to Self Test and Design Validation, Test Conference, 1998. Proceedings. International, 18-23 Oct 1998, Page(s): 990-999 □□
	V	Chen et al., Software-Based Self-Testing Methodology for Processor Cores, March 2001, Volume: 20 , Issue: 3, On page(s): 369 - 380
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.